## REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated February 16, 2007. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1-9 and 11 stand for consideration in this application, wherein claim 10 is being canceled without prejudice or disclaimer, while claims 1, 6, 7, and 11 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

Additional Amendments

The specification is being amended to correct formal errors. All amendments to the application are fully supported therein, including Fig. 5 and page 14, lines 4 – 8 of the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formal Objections

Title

The Examiner asserted that the Title of the Invention is not descriptive. Applicants respectfully disagree.

35 U.S.C. §112 does not require the Title be descriptive. Rather, 35 U.S.C. §112 sets forth that the specification shall contain a written description of the invention and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same. The Title of the Invention, which may be generally considered a part of the specification. Applicants respectfully submits that the present Title of the Invention describes the present invention as whole while the other part of the specification including written disclosure more specifically described the present invention, and therefore, meets the requirement of 35 U.S.C. §112.

Prior Art Rejections

The First 35 U.S.C. §102(e) rejection

Claims 1, 6, 10 and 11 were rejected under 35 U.S.C. §102(e) as being anticipated by Pinto et al. (U.S. 2004/0032952 A1). As mentioned above, claim 10 is being cancelled, and therefore, the rejection of claim 10 is moot. Applicants respectfully traverse the rejections of claims 1, 6 and 11 for the reasons set forth below.

According to the M.P.E.P. §2131, a claim is anticipated under 35 U.S.C. §102 (a), (b), and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Claim 1

Claim 1 as amended recites that a camera module of a lens integrated type comprises: a lens; an image sensor; and an image processing circuit, the image processing circuit comprising a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter, wherein said image processing circuit has correction means using, as a correction value, a value obtained by raising the distance from the central axis of an optical system including said lens to the second power to correct a light intensity corresponding to the pixel position of said image sensor.

An apparatus recited in claim 1 is directed to a camera module which is capable of performing shading correction by an electrical circuit. An image processing circuit recited in claim 1 comprises a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter. Fig. 5 illustrates an exemplary block diagram of these elements in the image processing circuit. The horizontal direction counter 1 indicates the coordinate in the horizontal direction by counting the number of pixels in the horizontal direction. The coordinate of the center position in the horizontal direction is set to the horizontal center position setting unit 2. The adder 3 obtains a difference from the values of the horizontal direction counter 1 and the horizontal center position setting unit 2. The absolute value converter 4 obtains an absolute value to compute the distance X from the optical axis in the horizontal direction. The vertical direction counter

5 indicates the coordinate in the vertical direction by counting the number of pixels (= the number of lines) in the vertical direction. The coordinate of the center position in the vertical direction is set to the vertical center position setting unit 6. The adder 7 obtains a difference between the value obtained by the vertical direction counter 5 and the value obtained by the vertical center position setting unit 6. The absolute value converter 8 obtains an absolute value to compute the distance Y from the optical axis in the vertical direction (Page 14, line 9 – page 15, line 2 of the specification). As such, the imaging processing circuit recited in claim 1 can easily compute the distance X from the optical axis in the horizontal direction and the distance Y from the optical axis in the horizontal direction.

In contrast, Pinto merely shows a processing circuit including a calculation circuit for modifying data of an image to compensate for shading effects. However, Pinto does not show or suggest either explicitly or implicitly that the processing circuit comprises a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter.

Therefore, Pinto does not show every element recited in claim 1. Accordingly, claim 1 is not anticipated by Pinto.

Claim 6, 11

Claims 6 and 11 have substantially the same features as those of claim 1, at least with respect to the processing circuit comprises a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter. As such, the arguments set forth above are equally applicable here. Claim 1 being allowable, claims 6 and 11 must also be allowable.

The First 35 U.S.C. §103(a) rejection

Claims 2-5 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Pinto in view of Niikawa (U.S. 2002/0135688 A1). This rejection is respectfully traversed for the reasons set forth below.

As set forth above, Pinto fails to teach all the elements recited in claim 1, from which claims 2-5 depend. The secondary reference of Niikawa shows an image processing apparatus comprises image acquiring part for acquiring a first image and a second image; a

shading corrector for performing a shading correction on each of the first image and the second image acquired by the image acquiring part; a position adjuster for performing positioning of the first image and the second image that have been subjected to the shading correction by the shading corrector; and an image generator for generating a synthesized image of the first image and the second image that have been subjected to the positioning by the position adjuster (Paragraph [0014]). Niikawa further shows that the shading correction circuit corrects the shading due to optical system with respect to the image data that has been subjected to A/D conversion. The shading correction circuit has a multiplier, and receives a timing control signal inputted from the timing control circuit and performs multiplication of image data converted in the A/D conversion circuit and a correction table inputted from the general controller (paragraph [0082]). However, Niikawa does not show or suggest that the image processing apparatus comprises a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter. In other words, the secondary reference of Niikawa fails to provide any disclosure, teaching or suggestion that make up for the deficiencies in Pinto. Therefore, at the time the invention was made, one of ordinary skill in the art would and could not embody all the features of the invention as recited in claim 1. Accordingly, claims 2-5, which depend from claim 1, are not obvious in view of all the prior art cited.

The Second 35 U.S.C. §103(a) rejection

Claims 7-9 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Niikawa in view of Nakamura (U.S. 2002/0008760 A1). This rejection is respectfully traversed for the reasons set forth below.

Claim 7 as amended recites that A camera module of a lens integrated type comprises: a lens; an image sensor; and an image processing circuit, the image processing circuit comprising a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter, wherein said image processing circuit has correction means using, as a correction value, a value obtained by multiplying a value obtained by raising the distance from the central axis of an optical system including said lens in the horizontal direction to the second power or a value obtained by raising the distance from the central axis of said optical system in the vertical direction to the

second power by a predetermined coefficient to correct a light intensity corresponding to the pixel position of said image sensor.

As set forth above, Niikawa does not show or suggest explicitly or implicitly that the image processing apparatus comprises a horizontal direction counter, a horizontal center position setting unit, a first adder, a first absolute value converter, a vertical direction counter, a vertical center position setting converter, a second adder, and a second absolute value converter.

The secondary reference of Nakamura fails to provide any disclosure, teaching or suggestion that make up for the deficiencies in Niikawa. Therefore, at the time the invention was made, one of ordinary skill in the art would and could not embody all the features of the invention as recited in claim 7. Accordingly, claim 7 is not obvious in view of all the prior art cited.

Claims 8-9

As to dependent claims 8-9, the arguments set forth above with respect to independent claim 7 are equally applicable here. The corresponding base claim being allowable, claims 8-9 must also be allowable.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

**REED SMITH LLP**
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

**July 12, 2007**
SPF/JCM/YOM